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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/405,618	09/24/1999	JAMES S. BLOMGREN	31876.0140	9689

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. 09/405,618

Art Unit 2123

The remand, paper # 15 has been responded to.

The Examiner respectfully requests that the following correction to the original Examiner's Answer be entered.

Please substitute old page 3 with the new page 3.

Summary

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dwin McTaggart Craig

Dwin McTaggart Craig
February 9, 2004

Conferees
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(9) Prior Art of Record

5,706,476	Giramma	1-1998
6,289,497	Leight et al.	11-2001

IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164), March 18, 1993, The Institute of Electrical and Electronics Engineers, Inc. New York, N.Y., ISBN 1-55937-299-0.

"On the Use of VHDL as a Multi-Valued Logic Simulator", C. Rozon, Royal Kings College, Kingston Ontario Canada, IEEE 1996.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

- **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claims 1-7, 8-14, 15-21, 22-28 and 29-35** in view of **Leight et al. U.S. Patent 6,289,497.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing a signal naming convention that describes an N-nary logic circuit. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have used the system as described in the *Leight et al.* reference to model signals in an N-nary logic simulation because, (...the tool of the present invention does not require a semiconductor designer to develop a schematic and a separate behavioral model that must be verified against each other. Instead, the design tool